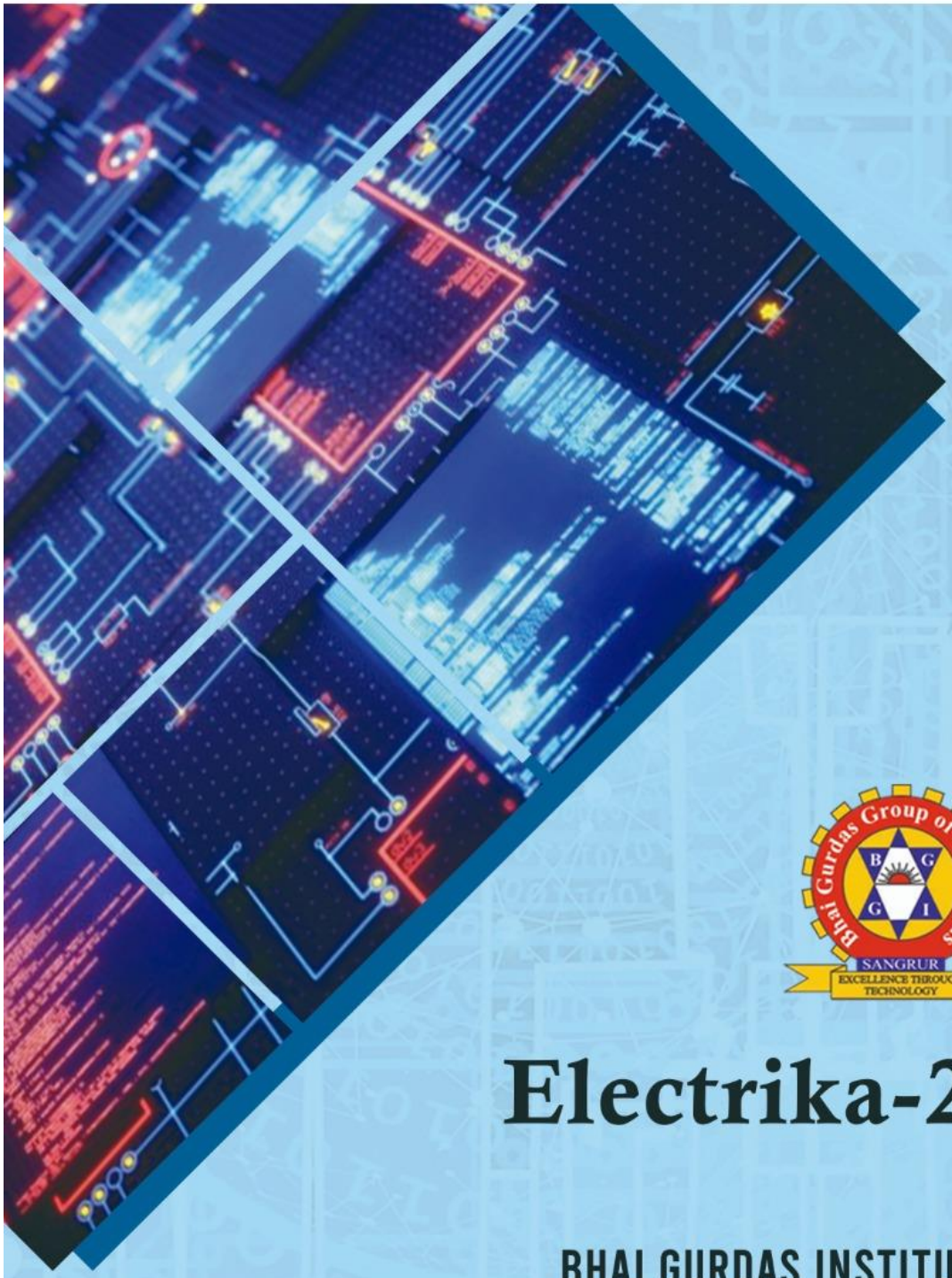
DEPARTMENT OF ELECTRICAL ENGINEERING



Electrika-20

BHAI GURDAS INSTITUTE OF ENGINEERING & TECHNOLOGY, SANGRUR

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I H.O.D EE hereby declare that the particulars given above are true to the best of my knowledge and belief.

Er. Sushil Kakkar

HOD Electrical Engineering

Dated 15 April 2020

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DIRECTOR'S MESSAGE

Dr. Tanuja Srivastava
Director, BGIET

It is matter of immense pleasure for me that the Electronics & Communication Department Engineering of BGIET, Sangrur committed to excellence through technology is going to launch Annual Magazine "Electrika-19". This will provide a common platform to Students, Faculty Members and Eminent Engineers to share their ideas and technological assets to translate innovations from basic knowledge to quality products for better returns and competitions at the global level. Besides it will encourage the young students for recognition of their new innovations and technologies at the Institute Level. I congratulate those students and Faculty Members who have contributed and urge other to avail the opportunity next time.

With Best Wishes
Dr. TanujaSrivastva

HOD's MESSAGE

Dear students,

It is a matter of great pride & happiness that the third edition of the Electronics magazine "Electrika-19" is in your hands. You are reading your own creative & technical output. It is an endeavor by the college to provide you with an opportunity to look beyond the mundane routine. I take this opportunity to thank the many people who have made this launch of the magazine possible. First and foremost are the authors of various articles and editorials whose works over the years have made the magazine a reality and I also thank the Publications Board and publications staff of this magazine who have extended themselves to make this magazine possible. Finally, I want to thank all of our readers both those who have been with us for many years and those who have only recently discovered the magazine. It always a pleasure when a reader comes up to me at Semi-Term or writes to me about how much they enjoy the magazine and how useful they have found one of the articles.

Keep it up. Wishing you good luck.

Dr. Sushil Kakkar

HOD Electrical Engineering

EE Department Activities

INDUCTION PROGRAM

Student Orientation Programme plays an important role in a student's transition to a college life. Orientation programmes are aimed at familiarizing the students to an unknown campus environment, its faculties and infrastructure. It helps them to find their way in the institute for the nextyears and also encourages them to get better adjusted to the institute environment. BGIET organized an 'Orientation Program' for newly admitted students every year, as it plays a significant role in introducing the institutions activities. During orientation, students were informed about the various cells and their activities, infrastructural facilities, extracurricular activities, learning resources, and the college culture. They were made to understand their role and responsibilities during college life. Therefore, in order to give the most accurate view of an institution, there must be both an academic and social component to the orientation program. Students were also informed about the rules & regulations, campus safety and the academic calendar. BGIET motivates the students and wished them Good Luck for their bright and glorious future.

INDUSTRIAL VISIT

Students of Electrical Engineering fourth and sixth semester visited an indusrty Crystal switchgear pvt ltd. Ludhiana. Our main purpose for this visit is to be familiar with industrial environment and to get practical knowledge of electrical power transmission and distribution Students of 4th semester will get the idea of electrical power transmission and distribution. Students will also get familiar with Transformer maintenance, circuit breaker, Transformer isolator, bus bar, Protective relays, Lightening arresters, Load break switches. Industrial visit provide practical exposure to students of course curriculum. It will enhance their knowledge by learning things physically.

TECHNICAL TALK

Seminar on “Advance Sensors and Smart Controllers” was organized by SEE society of Electrical Engineering department on 08/05/2019. The keynote speaker of the day was Er. Mani Bansal, Assistant Professor, DAVIET, JALANDHAR. He has shared his experience on Wireless Sensors those are utilized by the industries in present scenario. A total number of 93 students of electrical engineering department were participated in the workshop.

He said that by organizing 7th International Conference on Advancements in Engineering and Technology BGIET has motivated the young engineers to come ahead with their innovative ideas. Prof. A. P. Singh praised the efforts of the institution, researchers and students as through the participation in this conference they will have technical growth and help in the up-gradation

of the society and nation. He said that innovative approach leads to invention. Dr. Tanuja Srivastava (Director, BGIET) welcomed the Chief Guest, the Guests of Honor and the delegates from various national and international universities and hoped that the conference will provide a common and rewarding platform to the research scholars, where they can share their innovative ideas on advancements in Engineering and Technology. She further said that more than 192 research papers are received and about 200 delegates comprising eminent scientists, engineers, experts and research scholars participated in this conference. In this conference experts of national and international repute Dr. Anand Vaz, NIT Jalandhar, Dr. Monika Sogani, Manipal University Jaipur, Dr. Rajesh Khanna, Thapar University Patiala, Dr. Amit Mittal, Dean Research, Chitkara University, Dr. Jatinder Chabra, NIT, Kurukshetra, Dr. Poonam Jindal, NIT Kurukshetra graced the occasion with their presence.

WEBINAR ON PYTHON PROGRAMMING

Python is a high-level, general-purpose and a very popular programming language. Python programming language (latest Python 3) is being used in web development, Machine Learning applications, along with all cutting edge technology in Software Industry. Python Programming Language is very well suited for Beginners, also for experienced programmers with other programming languages like C++ and Java. Below are some facts about Python Programming Language: Python is currently the most widely used multi-purpose, high-level programming language. Python allows programming in Object-Oriented and Procedural paradigms. Python programs generally are smaller than other programming languages like Java. Programmers have to type relatively less and indentation requirement of the language, makes them readable all the time. Python language is being used by almost all tech-giant companies like – Google,

Amazon, Facebook, Instagram, Dropbox, Uber… etc. The biggest strength of Python is huge collection of standard library which can be used for the following:

- Machine Learning
- GUI Applications (like Kivy, Tkinter, PyQt etc.)
- Web frameworks like Django (used by YouTube, Instagram, Dropbox)
- Image processing (like OpenCV, Pillow)
- Web scraping (like Scrapy, BeautifulSoup, Selenium)
- Test frameworks
- Multimedia
- Scientific computing
- Text processing and many more..

WEBINAR ON IOT BASED INSTRUMENTS

IoT starts at the sensor level where pressure, level, flow, temperature, vibration, acoustic, position, analytical and other sensors collect data and send this collected information to control and monitoring systems via wired and wireless networks.

Over the last several years with the advent of sensors that are wireless, self-powered, non-intrusive, calibration free and maintenance free, production processes can now cost-effectively send information from thousands more sensors to the control and monitoring systems. These sensors help create the IoT for the facility and gives its operating and maintenance personnel a better understanding of overall plant operations.

These control and monitoring systems include distributed control systems (DCSs), asset management systems, enterprise resource planning (ERP) systems, and other specialized software such as vibration monitoring solutions. With expertise and strategic algorithms embedded into the control and monitoring systems, this creates understandable, actionable data for the right person via one of two basic methods: Collected information is presented to plant personnel and they decide what type of action to take Action is taken proactively

IEEE SPONSORED WEBINAR ON PUBLIC SPEAKING

Fear of public speaking is a common form of anxiety. It can range from slight nervousness to paralyzing fear and panic. Many people with this fear avoid public speaking situations altogether, or they suffer through them with shaking hands and a quavering voice. But with preparation and persistence, you can overcome your fear. Dr. Nazir Ahmad Mir, H&S Department of K.L University, Hyderabad shared his precious knowledge.

Global Positioning system

GLOBAL Positioning System (GPS) receivers for the consumer market require solutions that are compact, cheap, and low power. Manufacturers of cellular telephones, portable computers, watches, andother mobile devices are looking for ways to embed GPS into their products. Thus, there is a strongmotivation to provide highly integrated solutions at the lowest possible power consumption. GPS radiosconsist of a front-end and a digital. Base band section incorporating a digital processor. While for the baseband processor, cost-reductionreasons dictate the use of the densest digital CMOS technology, for the front-end, the best option interms of power consumption is a Si, Ge, Bi, CMOS technology. This explains why several commercial GPS radios consist of dual or multichip systems using the besttechnology option for the front-end and base band processor. On the other hand, the implementation of astand-alone GPS radio into a single chip in CMOS technology is appealing in terms of cost, and wouldspeed up the integration of GPS capabilities into mobile products. This motivated the development ofGPS macro blocks and radios in CMOS technology. However, the cost effectiveness of this solutiondepends on both reduction of external components and die area of the GPS radio. Since the silicon areaof RF CMOS circuits, including on-chip inductors, does not shrink at the same rate as technology scaling,the reduction of the total cost poses a severe challenge. This article describes the design andmeasurement of a fully integrated CMOS GPS receiver targeting active antenna applications with anarchitecture geared to highest integration and minimal silicon area at the lowest possible powerconsumption (i.e., comparable to the best ones available.

Architecture and Specifications

The GPS signal code is a direct-sequence spread spectrum, and the type of spread spectrum employedby GPS is known as binary phase-shift keying direct-sequence spread spectrum (BPSK DSSS). In aspread-spectrum system, data are modulated onto the carrier such that the transmitted signal has alarger bandwidth than the information rate of the data. The term "direct sequence" is used when thespreading of the spectrum is accomplished by phase modulation of the carrier. The GPS satellitesbroadcast signals in a 20 MHz-wide band (L1 band) centered at 1.575 GHz. Two DSSS signals arebroadcast in this band. They are known as the P code (or precision code) and the C/A code (or coarseFor the GPS C/A code channel, most of the signal energy is located in a 2-MHz band which lies at themiddle of the 20-MHz GPS-P code channel. At the antenna of a GPS receiver, the received signal poweris typically 130 dBm. In the 2-MHz main lobe of the C/A code, the noise power (KTB) is 111 dBm with anassociate signal-to-noise ratio (SNR) at the antenna of 19 dB. In the past, several architectures havebeen used to relax the constraints of the GPS receiver using off-chip filtering and external components.For instance, a dual-conversion architecture with a first IF between 100200 MHz and a second close to dcrelaxes the Constraints between selectivity and sensitivity of the receiver, i.e., allow using an externalfilter in front of the GPS low noise amplifier (LNA) with a lower quality factor. However, this comes with apenalty in terms of power consumption. IF section running at high frequency) or in terms of bill ofmaterials, since external IF filtering would be required. Another possibility is to use a single IF at a lowerfrequency with high quality factor off-chip RF filtering in front of the receiver. Clearly, the use of externalcomponents allows reducing the burden of the on-chip GPS receiver, and so its power consumption.Since we target a high level of integration, low-IF or zero-IF architecture with integrated IF filters must beselected. However, the presence of most of the energy at the center of the spectrum makes the use of azero-IF architecture for a CMOS implementation difficult, due to the presence of flicker noise. For this reason, a low-IF architecture with image rejection has been selected in order to relax constraints on theexternal RF filter and to reduce the noise figure (NF) of the receiver. The associate penalty is anincreased complexity and power consumption. An IF below 10 MHz guarantees a low energy at the imagefrequency and the feasibility of an integrated IF filters at a relatively low power consumption. Choosing an

IF of 9.45 MHz, the required rejection is about 30 dB.RF filters. This allows remote placement of theantenna from the receiver itself and relaxes noise requirements. A total voltage gain for the GPS receiverof 85 dB has been chosen. The combination of external LNA and GPS receiver brings the output signal(which is dominated by noise) to a level sufficiently high for the external analog-to-digital converter (ADC).For instance, if a 2-MHz band is considered, an external voltage gain between the antenna element andthe chip input of 20 dB (including losses associated with the

external filter and connectors) makes thetotal output noise power equal to -111dBm +105 dB~-6dBm. In order to reduce power consumption anddie area, the internal LNA uses a single-ended RF input. The LNAmixer combination has an input 1-dBcompression point (P1 dB) of 28 dBm; therefore, the use of a low-quality external RF filter is enough toprevent blocking of the receiver (RX) chain from UMTS and GSM carriers. The reported GPS radio down
converts the GPS L1 spread spectrum BPSK-modulated signal to an IF of 9.45 MHz (fully differentialoutputs) and provides two programmable CMOS.

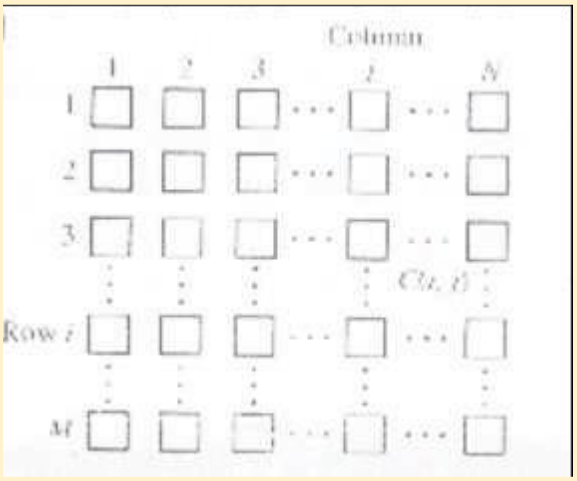
-Kiranjeet Kaur
EE-4th Sem.

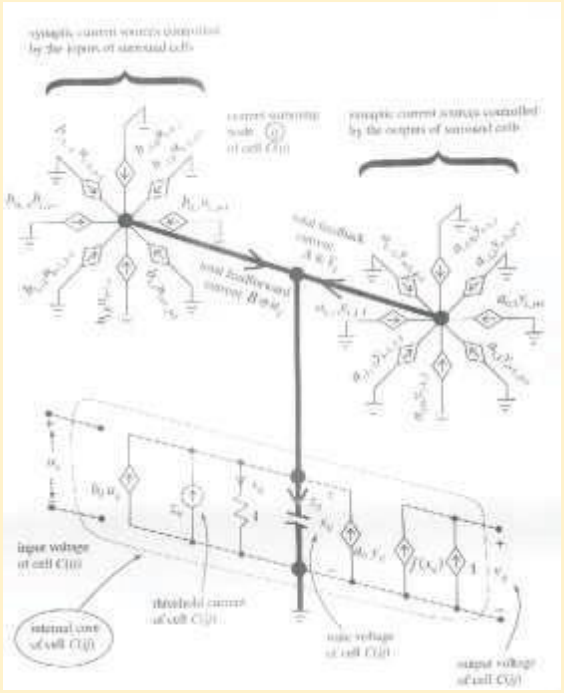
Cellular Neural Network

Cellular Neural Network is a revolutionary concept and an experimentally proven new computing paradigm for analog computers. Looking at the technological advancement in the last 50 years ; we seethe first revolution which led to pc industry in 1980's, second revolution led to internet industry in1990's cheap sensors &mems arrays in desired forms of artificial eyes, nose, ears etc. this thirdrevolution owes due to C.N.N. This technology is implemented using CNN-UM and is also used inimage processing.

ARCHITECTURE OF CNN

A standard CNN architecture consists of an m*n rectangular array of cells c(i, j) with Cartesiancoordinates (i,j) i=1,2.....M,j=12.....N.





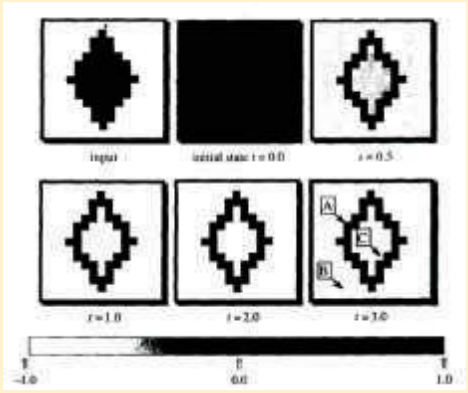
Voltage controlled current sources implement various coupling terms. These transconductances can beeasily constructed on "CMOS processing .It can also implementary Boolean functions.Voltage controlled current sources implement various coupling terms. These transconductances can beeasily constructed on "CMOS processing .It can also implementary Boolean functions.

CNN TEMPLATES

EDGE DETECTION TEMPLATE

Local rules

1. White pixel- white, independent of neighbours
2. Black pixel- white , if all nearest neighbours are black
3. Black pixel- black , if at least one nearest neighbour is white
4. Black, gray or white pixel-gray if nearest neighbours are gray



DIGITAL HARDWARE ACCELERATORS

We can emulate analog dynamics by digital hardware accelerators. Emulating large CNN arrays needmore computing power. A special hardware accelerator board (HAB) was developed for simulating up toone million pixel arrays with on board memory, with 4 DSP chips. Using hab's large arrays can besimulated with cheap pc. Actually the DSP is a reduced instruction set (RISC). Processor used forcalculating CNN dynamics New dsp packages host 4-8 dsp processors in a chip .hence the processnumbers are 4-8 times higher .since for the calculation of CNN dynamics ,a major part of dsp is notused a special purpose chip (castle) have been developed.

APPLICATIONS

1) Cheap sensors and mems arrays are in the desired forms of artificial eyes, nose, ears, taste & realization of telepathy.

2) High speed target recognition, tracking.

3) Real time visual inspection of manufacturing processes

4) In terms of speed, power, area this chip is far superior to any equivalent dsp implementation at least three orders of magnitude in either s ,p or a

5) intelligent vision capable of recognition of context-sensitive & moving scenes as well asapplications requiring real time fusing of multiple modalities such as multi spectral imagesinvolving infrared, long wave-infrared and polarized lights.

- Soni Rani

EE-6TH Sem

Digital Audio Broadcasting

Digital audio broadcasting, DAB, is the most fundamental advancement in radio technology since thatintroduction of FM stereo radio. It gives listeners interference free reception of CD quality sound, easy touse radios, and the potential for wider listening choice through many additional

stations and services.DAB is a reliable multi service digital broadcasting system for reception by mobile, portable and fixedreceivers with a simple, non-directional antenna. It can be operated at any frequency from 30 MHzto 3GHz for mobile reception (higher for fixed reception) and may be used on terrestrial, satellite, hybrid(satellite with complementary terrestrial) and cable broadcast networks. DAB system is a rugged, highspectrum and power efficient sound and data broadcasting system. It uses advanced digitalaudio compression techniques (MPEG 1 Audio layer II and MPEG 2 Audio Layer II) to achieve aspectrum efficiency equivalent to or higher than that of conventional FM radio. The efficiency of use ofspectrum is increased by a special feature called Single. Frequency Network (SFN). A broadcast networkcan be extended virtually without limit a operating all transmitters on the same radio frequency.

EVOLUTION OF DAB

DAB has been under development since 1981 of the Institute Fur Rundfunktechnik (IRT) andsince 1987 as part of a European Research Project (EUREKA-147).

In 1987 the Eureka-147 consortium was founded. Its aim was to develop and define the digitalbroadcast system, which later became known as DAB.In 1988 the first equipment was assembled for mobile demonstration at the Geneva WARCconference.

By 1990, a small number of test receivers was manufactured. They has a size of 120 dm3in 1992, the frequencies of the L and S band were allocated to DAB on a worldwide basis.From mid-1993 the third generation receivers, widely used for test purposes had a size of about 25dm3, were developed.The fourth generation JESSI DAB based test receivers had a size of about 3 dm3.1995 the first consumer type DAB receivers, developed for use in pilot projects, were presented atthe IFA in Berlin.In short

1992—1995 —field trial period.

1996 —1997— introduction period

98 onwards terrestrial services in full swing

For DAB via satellite 1996 2001 is planned as experimental stage 2002 2003 introduction period.

The conversion of analog audio data to the digital domain begins by sampling the audio input in regular,discrete intervals of time and quantizing the sampled values into a discrete number of evenly spacedlevels. The digital audio data consists of a sequence of binary values representing the number ofquantizer levels for each audio sample this method of representing each sample

with anindependent code word is called pulse code modulation (PCM).The digital representation of audio data offers many advantages.

- High noise immunity
- Stability
- Reproducibility
- Allows the efficient implementation of many audio processing functions (i.e. mixing, filtering, andequalization) though the digital computer.

According to the Shannon's theory, a time sampled signal can faith represent signal up to half the

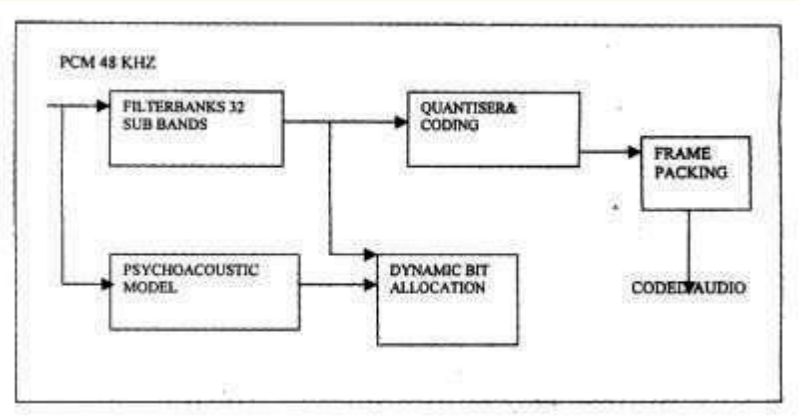
Sampling rate. The max audible frequency for humans is 20 KHz. Therefore the typical sampling rate is 48KHz. (i.e. more than twice the signal frequency).

DIGITAL AUDIO COMPRESSION

Digital audio compression allows the efficient storage andtransmission of audio data. While quantizing, the number of quantizer levels is typically a power of 2 tomake full use of a fixed no: of bits per audio sample to represent the quantized values. With uniformquantizer step spacing, each additional bit has the potential of increasing the signal to noise ratio. Thetypical number of bits per sample used for digital audio is 8, 16, 32, and 64. The audio data on a compactdisc (2 channels of audio samp1. at 44.1 KHz with 32 bits per sample) requires a data rate of32x2x44xl000 (megabits per second. Ti) transfer this uncompressed data requires a large data transferrate and a larger bandwidth. Therefore audio data need to be compressed for efficient storage andtransmission.

COMPRESSION TECHNIQUES The MPEG (Motion Picture Experts Group) audio compressionalgorithm is an International Standardization Organization (ISO) standard for high fidelity audiocompression. The high performance of this compression algorithm is due to the exploitation of auditorymasking. This masking is a perceptual weakness of the ear that occurs whenever the presence of astrong audio signal in spectral neighborhood of weaker audio signals makes it imperceptible. Thisnoise-masking phenomenon has been observed and corroborated through a variety of psychoacoustic experiments.Due to the Specific behavior of the inner ear, the human auditory system perceives only a small part of the complex audio spectrum. Only those parts of the spectrum located above the masking threshold ofa given sound contribute to its perception, whereas any acoustic action occurring at the same time butwith less intensity and thus situated under the masking threshold will not be heard because it is maskedby the main

sound event. To extract the perceptible part of the audio signal the spectrum is split into 32equally spaced sub-bands. In each sub-band the signal is quantized in such away that the quantizingnoise matches the masking threshold. This coding system for high quantity audio signals is known asMUSICAM (masking pattern adapted universal sub-band integrated coding and multiplexing)

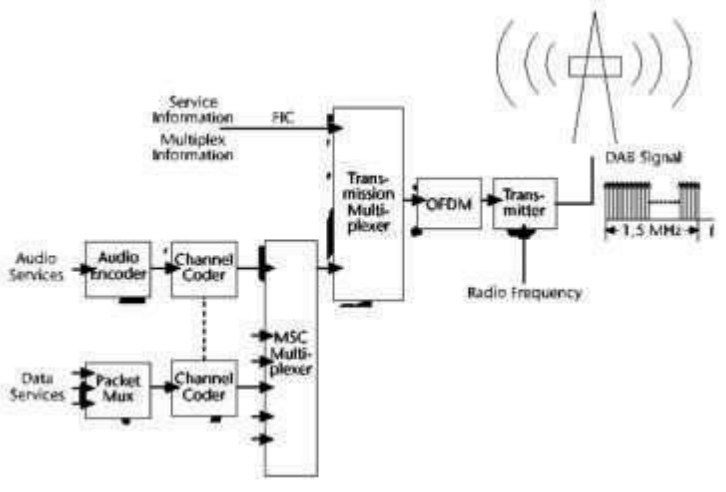


MUSICAM DAB CODER

The input audio stream passes through a filter bank that divides the input into multiple sub-bands. Theinput audio stream simultaneously passed though a psycho acoustic model that determines the signal-tomask ratio of each sub- band. The bit allocation block uses the signal-to mask ratios to decide how toapportion the total no: of code bits available for the quantization of the sub- signals to minimize theaudibility of the quantization noise. Finally, the last block takes the representation of the quantized audiosamples and formats the data into a decodable bit stream. The 32 constant width filter bands reflect theear's critical bands. With Kbs per stereo channel compared to 2,800 Kbs of CDs that use anuncompressed technique. MUSICAM, high quality audio can be perceived

OUT LINE OF THE DAB SYSTEMGENERATION OF DAB SIGNAL

The figure shows that block diagram of a conceptual DAB signal generator.



Conceptual DAB Signal Generator

Each service signal is coded individually at source level, error protected and time interleaved in thechannel codes. Then the services are multiplexed in the Main Service Channel (MSC), according to apredetermined, but adjustable, multiplex configuration. The multiplexer output is combined with multiplexcontrol and service information, which travel in the Fast Information Channel (FIC) to form thetransmission frames in the transmission multiplexer. Finally, Orthogonal Frequency Division Multiplexing(OFDM) is applied to shape the DAB signal which consists of a large number of carriers. The signal isthen transposed to the appropriate radio frequency band, amplified and transmitted. Thebroadcasting frequency for digital audio varies from 30 MHz3 GHz.

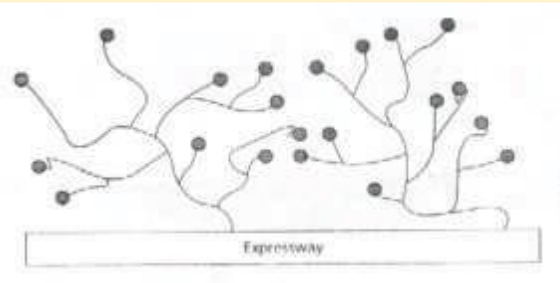
- Priyanka
EE-6th Sem

Distributed Wireless Networks

With the rapid progress in telecommunications, more and more services are provided on the basis ofbroadband communications, such as video services and high-speed Internet. With worldwidefundamental construction of a backbone network based on optical fiber providing almost unlimited

Communications capability, the limited throughput of the subscriber loop becomes one of the most Stringent bottlenecks. Compared to the capacity of the backbone network, which is measured by tensof gigabits per second, the throughput of the subscriber loop is much lower, only up to hundreds ofmegabits per second for wired systems (including fixed wireless access). However, for mobile access thethroughput is even lower, and depends on the mobility of the

terminal. For example, the peak data rate isonly 2 Mb/s for 3G systems. Since there will be more and more need for mobile services, the poorthroughput of mobile access not only limits user applications based on interconnection, but alsowastes the capability of the backbone network.This case is quite similar to the traffic conditions shown in Fig. a, which is an image of an ultra-wideexpressway with a few narrow entrances.



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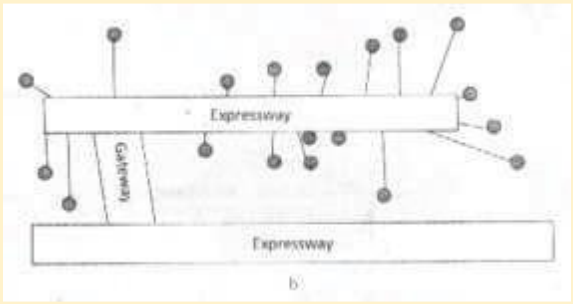


Since the little paths are rough, narrow, and crowded, the problems in Fig. a are:

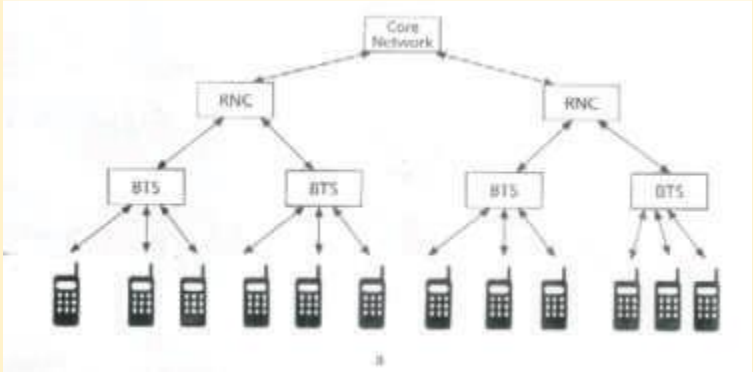
- Terminals are far away from the expressway, which will consume much power.
- Too many cars converge into the same narrow paths.
- Little paths converge several times before going into the expressway.
- The expressway is used insufficiently, since few cars are running on it.

In telecommunications, the optical fiber network(expressway)is relatively much cheaper than the Wireless spectrum (little paths), while the capability of the former is much greater than that of the later.As shown in Fig. b, besides the backbone expressway, there are some dedicated sub expressways usedto provide direct entrance for distributed subscribers. The above example implies that the high-capacitywired network, being so cheap, can help us solve the problem of wireless access(too many userscrowded in a very narrow bandwidth). The key issue is to provide each mobile user a direct or one-hopconnection to an optical network. This structure also follows

the trend in network evolution: thehierarchical or tree-like structure of traditional networks will be gradually flattened to simple single-layerones.

LOGIC STRUCTURE OF DWCS

For comparison, Fig. a shows the traditional tree structure of a cellular system, where each basetransceiver station (BTS) processes the signals to and from mobile terminals within its coverage, andconsiders the signals of other cells as interference. Terminals at the boundary of cells may hand offbetween adjacent BTSs, and the handoff is controlled by the radio network controller (RNC). When cellsize is reduced, hand-off frequency increases, and system overhead will be too heavy. Meanwhile,interference from other cells may become so strong that the capacity of each cell is very small. The basicidea of the distributed wireless communication system is to flatten.Such architecture, as indicated in Fig. b. The structure consists of three layers: distributedantennas, distributed signal processing, and distributed high-layer control.



DISTRIBUTED ANTENNAS

The new structure has a very high density of distributed antennas, so almostanywhere in the area may have a line of sight (LOS) to at least one fixed antenna. Each antenna isequipped with a transceiving device, which converts radio frequency (RF) to and from digital intermediatefrequency (IF) signals. The received IF signal is transmitted to the processing center through optical fiber.The IF signals for transmission and system timing are also provided by the processing center throughoptical fiber. Thus, we may have a large number of very low-cost transceivers with no informationloss introduced, since no base band signal processing is performed here.

DISTRIBUTED SIGNAL PROCESSING

This is the essential part of the architecture. All signal processingconcerning wireless access is involved in thislayer, including modulation / demodulation, channelcoding/decoding, joint detection, channel measurements, medium access control (MAC), link layer controltwo sub layers, distributed processing centers (DPCs) and the dedicated optical network. The opticalnetwork has

two main tasks: to collect and deliver digital IF signals to and from distributed antennas, andto connect the processing centers so that co-processing among different DPCs can be performedbased on High-speed real-time data exchange. The optical network may have any kind of topology star,bus, ring, or any other. Logically, this layer can be regarded as an extremely powerful processor (EPP),which connects all the RF modules of distributed antennas. This EPP is actually software radioequipment, and is realized by many workstations in parallel while exchanging data through a high speednetwork. With such a structure, the EPP knows all signals received from all antennas, and can control thetransmission of all the antennas. Thus, the whole system works like a point-to-multipoint system with alarge number of distributed antennas, which is actually a rather large-scale MIMO system. Practically,the coverage of signals from each terminal or distributed antenna is relatively small compared tothe whole area, so each processing center is responsible for the distributed antennas located nearby.

The regions for different processing centers may overlap each other; thus, co- processing must beinvolved. With a distributed processor, the system becomes scalable and software configurable. Thus,coexistence of difference systems, and system update and expansion may be quite easy.

DISTRIBUTED HIGH-LAYER CONTROL

This is also a logic layer, which may be performed on the sameplatform as signal processing. This layer performs all high-layer protocol control, including all signaling,switching, and mobility management (gateway to core network).

- Shruti Khanna
EE-6th Sem

Fram

Before the 1950's, ferromagnetic cores were the only type of random-access, nonvolatilememories available. A core memory is a regular array of tiny magnetic cores that can be magnetized inone of two opposite directions, making it possible to store binary data in the form of a magnetic field. Thesuccess of the core memory was due to a simple architecture that resulted in a relatively dense array ofcells. This approach was emulated in the semiconductor memories of today (DRAM's, EPROM's, andFRAM's). Ferromagnetic cores, however, were too bulky and expensive compared to the smaller, lowpowersemiconductor memories. In place of ferromagnetic cores ferroelectric memories are a goodsubstitute. The term “ferroelectric' indicates the similarity, despite the lack of iron in the materialsthemselves. Ferroelectric memory

exhibit short programming time, low power consumption andnonvolatile memory, making highly suitable for application like contact less smart card, digital cameraswhich demanding many memory write operations. In other word FRAM has the feature of both RAM andROM. A ferroelectric memory technology consists of a complementary metal-oxide-semiconductor(CMOS) technology with added layers on top for ferroelectric capacitors. A ferroelectric memory cell hasat least one ferroelectric capacitor to store the binary data, and one or two transistors that provide accessto the capacitor or amplify its content for a read operation.A ferroelectric capacitor is different from a regular capacitor in that it substitutes the dielectric witha ferroelectric material (lead zirconate titan ate (PZT) is a common material used)-when an electric field isapplied and the charges displace from their original position spontaneous polarization occurs anddisplacement becomes evident in the crystal structure of the material. Importantly, the displacement doesnot disappear in the absence of the electric field. Moreover, the direction of polarization can be reversedor reoriented by applying an appropriate electric field. A hysteretic loop for a ferroelectric capacitordisplays the total charge on the capacitor as a function of the applied voltage. It behaves similarly to that of a magnetic core, but for the sharp transitions around its coercive points, which implies that evena moderate voltage can disturb the state of the capacitor.

One remedy for this would be to modify a ferroelectric memory cell including a transistor in series with the ferroelectric capacitor. Called an access transistor, it woe control the access to thecapacitor and eliminate the need for a square like hysteresis loop compensating for the softness of the hysteresis loop characteristics and blocking unwanted disturb signals from neighboring memory cells. Once a cell is accessed for a read operation, its data are presented in the form of an anal signal toa sense amplifier, where they are compared against a reference voltage to determine the logic level.Ferroelectric memories have borrowed many circuit techniques (such as folded-bit linearchitecture) from DRAM's due to similarities of their cells and DRAM's maturity. Some architecturereviewed are,

- Wordline-parallel Plate line (WL//PL)
- Bit line-parallel Plate line (BL//PL)
- Segmented plate line (segmented PQ)
- Merged Wordline/Plate line architecture (ML)

BASIC MEMORY CELL STRUCTURE

A ferroelectric memory cell, known as IT- IC (one transistor, one capacitor), structure which issimilar to that of DRAM. The difference is that ferroelectric film is used as its storage capacitor ratherthan Para electric material as in DRAM.

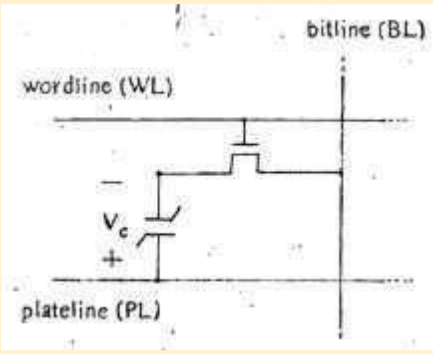


Fig. 1. Ferroelectric IT-IC structure

Figure above shows memory cell structure, consists of a single ferroelectric capacitor that isconnected to a Plate line(PL) at one end and, via an access transistor, to a Bit line(BL) at the other end.Raising the word line (WL) and hence turning ON the access transistor accesses the cell.As shown in fig 2 ferroelectric memory technology consists of a CMOS technology with added layers on top for ferroelectric capacitors. Therefore, by masking parts of the design that are not using ferroelectric capacitors, CMOS digital and analog circuits can be integrated together withferroelectric memories, all in the same chip. Ferroelectric capacitors to sit directly on the top of thetransistors by means of stacked vias, hence reducing cell area.

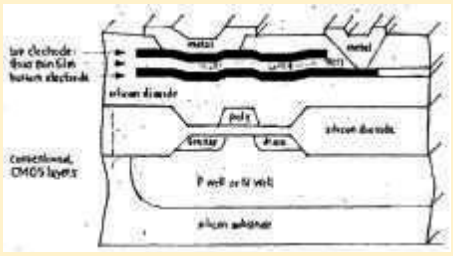


Fig. 2. Ferroelectric Capacitor layers on top of conventional CMOS process

BASIC MEMORY CELL OPERATION

The principles of operation of ferroelectric capacitor and ferromagnetic core are similar. We firstdiscuss the principle of operation of ferromagnetic memories, which make it easier to understand theoperation of ferro electric cell.

FERROMAGNETIC CORE

A core memory, as shown in Fig. 3, consists of a regular array of tiny magnetic cores that can be magnetized in one of two opposite directions, hence storing binary data in the form of a magnetic field. Awrite access into a core consists of sending simultaneous current pulses through the core via its xaccessand y-access wires. Depending on the directions of the current pulses, a core is magnetized in a"0" or a "1" direction. The basic assumption here is that only the core that receives two simultaneous current pulses is affected. All the remaining cores, including those that receive one current pulse or none,retain their original magnetization.A core memory, as shown in Fig. 2, consists of a regular array of tiny magnetic cores that can bemagnetized in one of two opposite directions, hence storing binary data in the form of a magnetic field. Awrite access into a core consists of sending simultaneous current pulses through the core via its xaccessand y-access wires. Depending on the directions of the current pulses, a core is magnetized in a"0" or a "1" direction. The basic assumption here is that only the core that receives two simultaneous current pulses is affected. All the remaining cores, including those that receive one current pulse or none,retain their original magnetization.

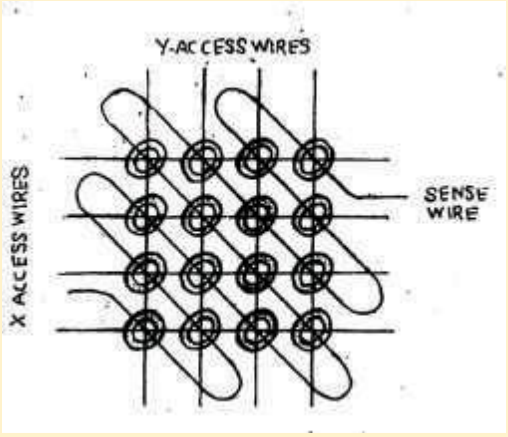


Fig. 2. Two-dimension array of Ferroelectric

- Kaushal
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Compact Peripheral Component Interconnect

Compact peripheral component interconnect (CPCI) is an adaptation of the peripheral componentinterconnect (PCI) specification for industrial computer applications requiring a

smaller, morerobust mechanical form factor than the one defined for the desktop. Compact PCI is an openstandard supported by the PCI Industrial Computer Manufacturer's Group (PICMG). Compact is bestsuited for small, high-speed industrial computing applications where transfers occur between a number ofhigh-speed cards. It is a high-performance industrial bus that uses the Euro card form factor and is fullycompatible with the Enterprise Computer Telephony Forum(ECTF) computer telephony (CT) Bus™H.110 standard specification. Compact PCI products make it possible for original equipmentmanufacturers (OEM), integrators, and resellers to build powerful and cost-effective solutions fortelco networks, while using fewer development resources. Compact PCI products let developersscale their applications to the size, performance, maintenance, and reliability demands of telcoenvironments by supporting the CT Bus, hot swap, administrative tools such as simple networkmanagement protocol (SNMP), and extensive system diagnostics. The move toward open, standardsbasedsystems has revolutionized the computer telephony (CT) industry. There are a number ofreasons for these changes. Open systems have benefited from improvements in personal computer (PC)hardware and software, as well as from advances in digital signal processing (DSP) technology. As aresult, flexible, high performance systems are scalable to thousands of ports while remaining costeffective for use in telco networks. In addition, fault-tolerant chassis, distributed software architecture, and N+1 redundancy have succeeded in meeting the demanding reliability requirements of network operators.One of the remaining hurdles facing open CT systems is serviceability. CT systems used in publicnetworks must be extremely reliable and easy to repair without system downtime. In addition, networkoperation requires first-rate administrative and diagnostic capabilities to keep services up and running.

The Compact PCI Standard

The Peripheral Component Interconnect Industrial Computer Manufacturer's Group (PICMG) developed the compact peripheral component interconnect (CompactPCI) specification in 1994. CompactPCI is ahigh-performance industrial bus based on the peripheral component interconnect (PCI) electricalstandard. It uses the Euro card form factor first popularized by Versa Module-Eurocard (VME). Compared to the standard PCI desktop computer, Compact PCI supports twice as many PCI slots (eight) on a singlesystem bus. In addition, CompactPCI boards are inserted from the front of the chassis and can routeinput/output (I/O) through the backplane to the back of the chassis. These design considerations makeCompact PCI ideal for telco environments.

Features	VME	CompactPCI	PCI	ISA
Address Space (Physical)	4GB	4GB	4GB	1 or 16MB
Addressing	Geographic	Slot Sensitive or	Slot Sensitive	Board locator technology (BLT)
CPUs in	Multiple	1(Master)	1(Master)	1
Hot Swap	VITA 1.4-100	PICMG hotswap	PCISIG hotplug	Not supported
System	40-80 Mbps	132 Mbps	132 Mbps	8 Mbps

Fundamental Components

CompactPCI offers a substantial number of benefits for developers interested in building telco-gradeapplications.CompactPCI systems offer the durability and maintainability required for network applications. At thesame time, they can be built using standard, off-the-shelf components and can run almost any operating system andthousands of existing software applications without modification. Other advantages of CompactPCI are related to itsEuro card form factor, durable and rugged design, hot swap capability, and compatibility with the CT Bus.

CompactPCI Features

- CompactPCI devices are fully compliant with PCI rev. 2.0.
- CompactPCI uses standard PCI chip sets.
- CompactPCI uses passive backplane architecture.
- CompactPCI is processor independent.
- CompactPCI provides plug-and-play facilities.
- CompactPCI uses an industrial card format.
- CompactPCI uses a high-density pin and socket connector.
- CompactPCI maximizes the number of PCI slots

The PCI Advantage

The PCI bus has been defined by Intel as a local bus providing an ultra-fast direct link between the CPU and high speedperipherals devices. PCI has been adopted by every CPU manufacturer and is at the core of all modern IntelPentium, Digital Equipment Corporation (DEC) Alpha, and IBM/Motorola PowerPC systems.High Performance

- 32-bit and 64-bit bus with peak bandwidth at 264 Mbps
- concurrent processing with processor/memory subsystems
- Synchronous bus operation at a 25 to 33 MHz clock

- Low power consumption (5V or 3.3V technology)
- Low Cost
- Easy to Use
- PCI peripheral boards contain configuration for automatic plug-and play
- PCI bus topology can be expanded using transparent PCItoPCI bridges
- Hidden overlapped central arbitration
- Broad operating system and application software support
- Industrial Form Factor

Industrial computers must be capable of operating reliably in the most demanding environment. They shouldtolerate heat, dirt, and high shocks and vibrations, with meantime between failures (MTBF) measured in tens ofthousands of hours. CompactPCI defines a single or double Eurocard (3U or 6U) board format. Boards mountvertically for best cooling characteristics, with card extractors and user I/O connectors in the front of thecard. CompactPCI uses a standard Euro card chassis available from many vendors.

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Crusoe Processor

Mobile computing has been the buzzword for quite a long time. Mobile computing devices like laptops,web slates & notebook PCs are becoming common nowadays. The heart of every PC whethera desktop or mobile PC is the microprocessor. Several microprocessors are available in the market for desktop PCs from companies like Intel, AMD, and Cyrix etc.The mobile computing market has never hada microprocessor specifically designed for it. The microprocessors used in mobile PCs are optimizedversions of the desktop PC microprocessor. Mobile computing makes very different demands onprocessors than desktop computing, yet up until now, mobile x86 platforms have simply made do with thesame old processors originally designed for desktops. Those processors consume lots of power, and theyget very hot. When you're on the go, a power-hungry processor means you have to pay a price: run out ofpower before you've finished, run more slowly and lose application performance, or run through theairport with pounds of extra batteries. A hot processor also needs fans to cool it; making the resulting mobile computer bigger, clunkier and noisier. A newly designed microprocessor with low powerconsumption will still be rejected by the market if the performance is poor. So any attempt in this regardmust have

a proper 'performance-power' balance to ensure commercial success. A newly designed microprocessor must be fully x86 compatible that is they should run x86 applications just like conventionalx86 microprocessors since most of the presently available software's have been designed to work on x86platform. Crusoe is the new microprocessor which has been designed specially for the mobilecomputing market. It has been designed after considering the above mentioned constraints. Thismicroprocessor was developed by a small Silicon Valley startup company called Transmeta Corp. afterfive years of secret toil at an expenditure of $100 million. The concept of Crusoe is well understood fromthe simple sketch of the processor architecture, called 'amoeba'. In this concept, the x86-architecture isan ill-defined amoeba containing features like segmentation, ASCII arithmetic, variable-length instructionsetc. The amoeba explained how a traditional microprocessor was, in their design, to be divided up intohardwareand software.Thus Crusoe was conceptualized as a hybrid microprocessor that is it has a software part and ahardware part with the software layer surrounding the hardware unit. The role of software is toact as an emulator to translate x86 binaries into native code at run time. Crusoe is a 128-bitmicroprocessor fabricated using the CMOS process. The chip's design is based on a technique calledVLIW to ensure design simplicity and high performance. Besides this it also uses Transmeta's twopatented technologies, namely, Code Morphing Software and Longrun Power Management. It is ahighly integrated processor available in different versions for different market segments.

Technology Perspective

The Transmeta designers have decoupled the x86 instruction set architecture (ISA) from the underlyingprocessor hardware, which allows this hardware to be very different from a conventional x86implementation. For the same reason, the underlying hardware can be changed radically without affectinglegacy x86 software: each new CPU design only requires a new version of the Code Morphing softwareto translate x86 instructions to the new CPU's native instruction set. For the initial Transmeta products,models TM3120 and TM5400, the hardware designers opted for minimal space and power. Byeliminating roughly three quarters of the logic transistors that would be required for an all-hardwaredesign of similar performance, the designers have likewise reduced power requirements and die size.However, future hardware designs can emphasize different factors and accordingly use differentimplementation techniques. Finally, the Code Morphing software which resides in standard FlashROMs itself offers opportunities to improve performance without altering the underlying hardware.

CRUSOE PROCESSOR ARCHITECTURE

The Crusoe microprocessor is available in the market in the following versions: TM3120, TM3200,TM5400 and TM5600. The basic architecture of all the above models is same except for some minorchanges since various models have been introduced for different segments of the mobile computing market. The following architectural description has taken Crusoe TM5400 as reference. The CrusoeProcessor incorporates integer and floating point execution units, separate instruction and datacaches, a level-2 write-back cache, memory management unit, and multimedia instructions. Inaddition to these traditional processor features, the device integrates a DDR SDRAM memory controller,SDR SDRAM memory controller, PCI bus controller and serial ROM interface controller. These additional units are usually part of the core system logic that surrounds the microprocessor. The VLIWprocessor, in combination with Code Morphing software and the additional system core logic units,allow the Crusoe Processor to provide a highly integrated, ultra-low power, high performance platformsolution for the x 86 mobile markets.

Processor Core

The Crusoe Processor core architecture is relatively simple by conventional standards. It is basedon aVery Long Instruction Word (VLIW) 128-bit instruction set. Within this VLIW architecture, the control logicof the processor is kept very simple and software is used to control the scheduling of instructions. Thisallows a simplified and very straightforward hardware implementation with an in-order 7- stage integerpipeline and a 10-stage floating point pipeline. By streamlining the processor hardware and reeducatecontrol logic transistor count, the performance-to-power consumption ratio can be greatly improved overtraditional x86 architectures. The Crusoe Processor includes a 8-way set-associative Level 1 (L1)instruction cache, and a 16-way set associative L1 data cache. It also includes an integratedLevel 2 (L2) write-back cache for improved effective memory bandwidth and enhanced performance.This cache architecture assures maximum internal memory bandwidth for performance intensive mobileapplications, while maintaining the same low-power implementation that provides a superior performanceto-power consumption ratio relative to previous x86 implementations. Other than having executionhardware for logical, arithmetic, shift, and floating point instructions, as in conventional processors,the Crusoe Processor has very distinctive features from traditional x86 designs. To ease the translationprocess from x86 to the core VLIW instruction set, the hardware generates the same conditioncodes as conventional x86 processors and operates on the same 80-bit floating point numbers. Also, theTranslation Look-aside Buffer (TLB) has the same protection bits and address mapping as x86processors. The software component of this

solution is used to emulate all other features of the x86architecture. The software that converts x86 programs into the core VLIW instructions is the CodeMorphing software.

FEATURES OF VARIOUS CRUSOE PROCESSORS

Crusoe Processor Model TM3200 Features

- VLIW processor and x86 Code Morphing software provide x86-compatible mobile platformsolution.
- Processor core operates at 366 and 400 MHz.
- Integrated 64K-byte instruction cache and 32K-byte data cache.
- Integrated north bridge core logic features facilitate compact system designs.
- SDR SDRAM memory controller with 66-133 MHz, 3.3V interface.
- PCI (Peripheral Component Interface) bus controller (PCI 2.1 compliant) with 33 MHz, 3.3V interface.
- Advanced power management features and very-low power operation extend mobile battery life
- Full System Management Mode (SMM) support.

CONCLUSION

In 1995, Transmeta set out to expand the reach of microprocessors into new markets by dramaticallychanging the way microprocessors are designed. The initial market is mobile computing, in whichcomplex power-hungry processors have forced users to give up either battery running time orperformance. The Crusoe processor solutions have been designed for lightweight (two to four pound)mobile computers and Internet access devices such as handhelds and web pads. They can give thesedevices PC Capabilities and unplugged running times of up to a day. To design the Crusoe processorchips, the Transmeta engineers did not resort to exotic fabrication processes. Instead they rethought thefundamentals of microprocessor design. Rather than “throwing hardware” at design problems, they chosean innovative approach that employs a unique combination of hardware and software. Using software todecompose complex instructions into simple atoms and to schedule and optimize the atoms for parallelexecution saves millions of logic transistors and cuts power consumption on the order of 60-70%over conventional approacheswhile at the same time enabling aggressive code optimization techniquesthat are simply not feasible in traditional x86 implementations. Transmeta's Code Morphing software and fast VLIW hardware, working together, achieve low power consumption without sacrificing highperformance for real-world applications. Although the model TM3120 and

model TM5400 are impressivefirst efforts, the significance of the Transmeta approach to microprocessor design is likely to become moreapparent over the next several years. The technology is young and offers more freedom to innovate(both hardware and software) than conventional hardware-only designs. Nor is the approach limited tolow-power designs or to x86-compatible processors. Freed to render their ideas in a combination ofhardware and software, and to evolve hardware without breaking legacy code, Transmeta microprocessordesigners may produce one surprise after another in the coming years.

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Intrusion Detection

In the last three years, the networking revolution has finally come of age. More than ever before, we seethat the Internet is changing computing as we know it. The possibilities and opportunities are limitless;unfortunately, so too are the risks and chances of malicious intrusions. It is very important that thesecurity mechanisms of a system are designed so asto prevent unauthorized access to system resourcesand data. However, completely preventing breaches of security appear, at present, unrealistic. We can,however, try to detect these intrusion attempts so that action may be taken to repair the damagelater. This field of research is called Intrusion De tection.Anderson, while introducing the concept ofintrusion detection in 1980, defined an intrusion attempt or a threat to be the potential possibility of adeliberate unauthorized attempt toAccess information, manipulate information, or render a system unreliable or unusable. Since then, several techniques for detecting intrusions havebeen studied. This article discusses why intrusion detection systems are needed, the main techniques,present research in the field, and possible future directions of research.

SECURITY POLICY

A Security Policy defines what is permitted and what is denied on a system. There are two basicphilosophies behind any security policy:

1. Prohibitive where everything that is not expressly permitted is denied.
2. Permissive where everything that is not expressly denied is permitted.

Elements of a System's Security

A computer system can be considered as a set of resources which are available for use byauthorized users. There are six elements of security that must be addressed by a security administrator. Itis worth evaluating any tool by determining how it addresses these six elements.

1. Availability - the system must be available for use when the users need it. Similarly, critical datamust be available at all times.

2 Utility - the system, and data on the system, must be useful for a purpose.

3. Integrity the system and its data must be complete, whole, and in a readable condition.

4. Authenticity - the system must be able to verify the identity of users, and the users should beable to verify the identity of the system.

5. Confidentiality - private data should be known only to the owner of the data, or to a chosen fewwith whom the owner shares the data.

6. Possession - the owners of the system must be able to control it. Losing control of a systemto amalicious user affects the security of the system for all other users.

The need for Intrusion Detection Systems

A computer system should provide confidentiality, integrity and assurance against denial of service.However, due to increased connectivity (especially on the Internet), and the vast spectrum of financialpossibilities that are opening up, more and more systems are subject to attack by intruders. Thesesubversion attempts try to exploit flaws in the operating system as well as in application programs andhave resulted in spectacular incidents like the Internet Worm incident of 1988.There are two ways tohandle subversion attempts. One way is to prevent subversion itself by building a completely securesystem. We could, for example, require all users to identify and authenticate themselves; we couldprotect data by various cryptographic methods and very tight access control mechanisms. Howeverthis is not really feasible because:

1. In practice, it is not possible to build a completely secure system because bug freesoftware is still a dream, & no-one seems to want to make the effort to try to develop suchsoftware. Apart from the fact that we do not seem to be getting our money's worth when we buysoftware, there are also security implications when our E-mail software, for example, can beattacked. Designing and implementing a totally secure system is thus an extremely difficult task.

2. The vast installed base of systems worldwide guarantees that any transition to secure system,(if itis ever developed) will be long in coming.

3. Cryptographic methods have their own problems. Passwords can be cracked, users can lose theirpasswords, and entire crypto-systems can be broken.

4. Even a truly secure system is vulnerable to abuse by insiders who abuse their privileges?

5. It has been seen that that the relationship between the level of access control and userefficiency is an inverse one, which means that the stricter the mechanisms, the lower the efficiency
becomes. .

We thus see that we are stuck with systems that have vulnerabilities for a while to come. If thereare attacks on a system, we would like to detect them as soon as possible (preferably in real-time) andtake appropriate action. This is essentially what an Intrusion Detection System (IDS) does. An IDS doesnot usually take preventive measures when an attack is detected; it is a reactive rather than proactiveagent. It plays the role of an informant rather than a police officer. The most popular way to detect intrusions has been by using the audit data generated by the operating system. An audit trail is a recordof activities on a system that are logged to a file in chronologically sorted order. Since almost allactivities are logged on a system, it is possible that a manual inspection of these logs would allowintrusions to be detected. However, the incredibly large sizes of audit data generated (on the orderof 100 Megabytes a day) make manual analysis impossible. IDS automate the drudgery of wadingthrough the audit data jungle. Audit trails are particularly useful because they can be used to establishguilt of attackers, and they are often the only way to detect unauthorized but subversive user activity.Many times, even after an attack has occurred, it is important to analyze the audit data so that theextent of damage can be determined, the tracking down of the attackers is facilitated, and steps maybe taken to prevent such attacks in future. An IDS can also be used to analyze audit data for suchinsights. This makes IDS valuable as real-time as well as post-mortem analysis tools. Anderson alsoclassified intruders into two types, the external intruders who are unauthorized users of the machinesthey attack, and internal intruders, who have permission to access the system, but not some portionsof it. He further divided internal intruders into intruders who masquerade as another user, those withlegitimate access to sensitive data, and the most dangerous type, the clandestine intruders, who havethe power to turn off audit control for themselves.

Classification of Intrusion Detection Systems

Intrusions can be divided into 6 main types

1. Attempted break-ins, which are detected by a typical behavior profiles or violations of securityconstraints.

2. Masquerade attacks, which are detected by a typical behavior profiles or violations of securityconstraints.

3. Penetration of the security control system, which are detected by monitoring for specificpatterns of activity.

4. Leakage, which is detected by atypical use of system resources.

5. Denial of service, which is detected by atypical use of system resources.

6. Malicious use, which is detected by atypical behavior profiles, violations of security constraints, oruse of special privileges.

Conclusion:

Intrusion Detection is still a fledgling field of research. However, it is beginning to assumeenormous importance in today's computing environment. The combination of facts such as theunbridled growth of the Internet, the vast financial possibilities opening up in electronic trade, andthe lack of truly secure systems make it an important and pertinent field of research. Futureresearch trends seem to be converging towards a model that is a hybrid of the anomaly and misusedetection models; it is slowly acknowledged that neither of the models can detect all intrusion attempts ontheir own. This approach has been successfully adopted in NIDES, and we can expect more suchattempts in the future.

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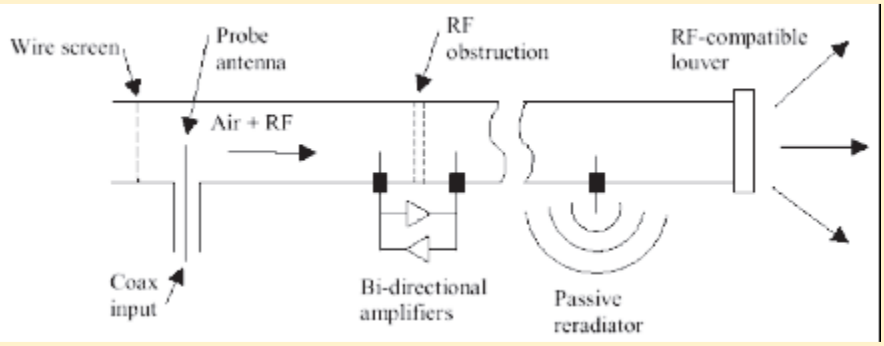
HVAC

Wireless transmission of electromagnetic radiation (communication signals) has become a popular method of transmitting RF signals such as cordless, wireless and cellular telephone signals, paper signals, two way radiosignals, video conferencing signals and LAN signals indoors. Indoor wireless transmission has the advantage thatbuilding in which transmission is taking place does not have to be filled with wires or cables that are equipped tocarry a multitude of signals. Wires and signals are costly to install and may require expensive upgrades when theircapacity is exceeded or when new technologies require different types of wires and cables than those alreadyinstalled. Traditional indoor wireless communication systems transmit and receive signals through the useof a network of transmitters, receivers and antennas that are placedthrough out the interior of a building.Devices must be located such that signals must not be lost or signal strength may not get attenuated. Againa change in the existing architecture also affects the wireless transmission. Another challenge related to installationof wireless networks in buildings is the need to predict the RF propagation and coverage in the presence of complexcombinations of shapes and materials in the buildings.In general, the attenuation in buildings is larger than that in free space, requiring more cells

and higher power toobtain wider coverage. Despite of all these, placement of antennas, rEEivers and antennas in an indoorenvironment is largely a process of trial and error. Hence there is need for a method and a system for efficientlytransmitting RF and microwave signals indoors without having to install an extensive system of wires and cablesinside the buildings.

THE HVAC SYSTEM

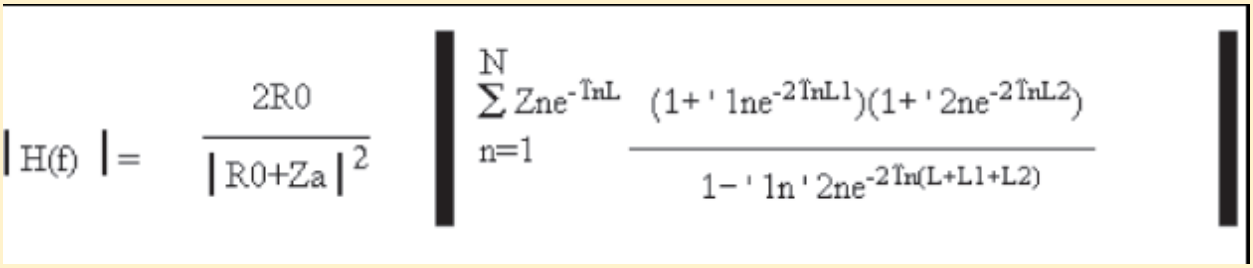
Heating, Ventilation and Air Conditioning are ducts used in buildings designed to carry air to and from all parts of thebuilding. In most parts of the USA and Europe almost every building is equipped with these HVAC ducts which canalso function as hollow wave guides for microwave and RF signals. Therefore, all forms of wireless transmission canin principle can be done through these waveguides. Since most of the offices and other places in buildings wherepeople work, sit or reside are reached by this HVAC ductwork, it is also possible to provide communicationsbetween building occupants and rest of the world. The HVAC system includes a device usually a coupler forintroducing electromagnetic radiation into the duct work such that the duct acts as a wave guide. System alsoincludes devices for enabling the electromagnetic radiation to propagate beyond the duct. In most cases ducts arelargest near the central air handling equipment and become smaller as they branch out to various rooms. Branchesin the duct behave as wave guide power splitters. Eventually RF would be radiated into the rooms through speciallydesigned louvers. Coverage in corridors and spaces guarded from louvers could be realized by placing passivereradiates in the sides of the ducts.



PROPAGATION MODEL

The HVAC channel like all other wave guides is a linear channel and therefore can be completely characterizedby its frequency response or transfer function. To design a wireless HVAC system, an analytic model isnecessary. This model must be valid for the ducts of different cross sections and allow to investigate easily thefrequency response dependence on such parameters as antenna geometry, transmitter receiver separationdistance, duct cross section size, conductivity of duct material, reflection coefficients of terminated duct endsetc. Such a model for the HVAC duct channel in the case of a straight multimode duct terminated at both ends isgiven below.This is a straight HVAC duct of circular cross-section, made of metal and and terminated at each end as shown. Twomonopole probe antennas provide

the coupling. Such a duct is a double-probe wave guide with a number ofpropagating modes N determined by the operating frequency and waveguide dimensions. Let the terminationloads 1&2 ie load1 and load2, have respective reflection coefficients '1n & '2n for wave guide of mode nwhich can be frequency dependent. Let 'L' be the distance between the two antennas and respective distances tothe terminated ends be L1 and L2.then theoretically the frequency response can be derived as



where 'Ro' is the internal impedance of transmitter or rEEiver; 'Za' the antenna impedance; 'Zn' the impedance dueto mode n; '¡n' the propagation constant.

CONCLUSTION

This article presents a new technique for high speed communication inside buildings which seems to a viableinexpensive alternative to other existing "last mile" technologies. Because existing infrastructure is used and theducts exhibit losses that are low compared with direct propagation and leaky coax, such a system has thepotential to be lower in cost and more efficient than either conventional method. An approximate, closed-form,propagation model for the straight HVAC duct channel in the form of a multimode wave guide is presented here.Experimental measurements are performed to validate this model and they are found to confirm the theoreticalresults. Efficient modeling of RF propagation in a real HVAC system is a challenging task. However this modelshould be perceived as a first step toward predicting the radio coverage in ducts when designing an HVAC wirelessdistribution system.

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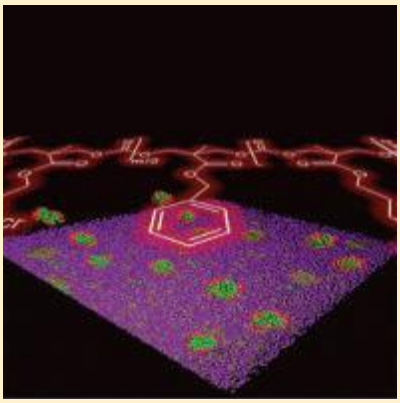
Using Nanotech to Fight Drug-Resistant Bacteria



BACTERIA BUSTERS: Researchers from IBM and the Institute of Bioengineering and Nanotechnologydiscovered a nanomedicine breakthrough in which new types of polymers were shown to physicallydetect and destroy antibiotic-resistant bacteria and infectious diseases like Methicillin-resistantStaphylococcus aureus, known as MRSA. Image: COURTESY OF IBM RESEARCH Antibiotics haveproved to be a valuable weapon in the fight against infection, but their popularity has also become theirundoing. Although the drugs cripple harmful microbes from within, bacteria that survive such sabotagetend to dangerous. To counter this, a team of researchers led by IBM Researchlmaden in San Jose,Calif., and Singapore's Institute are developing a technique that enlists polymer-based nanoparticles tosupplement antibiotics by destroying bacteria protective membranes, ensuring that their morphing daysare through. Just as important, upon completing their mission these Nan assassins would biodegradeharm lessly within the body. Drug resistance develops in part because conventional antibiotics such asciprofloxacin and doxycycline do not physically damage a microbe's cell wall. Instead, they enter theirtarget less disruptively and move on to disrupt the DNA within or block cell division or trigger cellular self-destruction. Strains that survive this assault, however, can evolve to defend themselves against futureattacks, opening the door for deadlier versions of bacteria such as methicillin-resistant Staphylococcusaureus (MRSA), which killed nearly 19,000 Americans in 2005 (the last year for which the U.S. Centersfor Disease Control has comprehensive data).In addition, the high doses of antibiotics needed to kill suchan infection indiscriminately destroyHealthy red blood cells in addition to contaminated ones. "This whole issue of emerging resistance ofantibiotics is going to be a huge problem in the foreseeable future," says James Hedrick, the IBMResearch advanced organic materials scientist who led the study, published April 4 in Nature Chemistry(Scientific American is part of Nature Publishing Group). "I think we can start to see it now with thenumber of infections, associated deaths and health care costs."Hedrick and his colleagues propose atandem that deploys biodegradable nanostructuresperhaps injected directly

into the body or appliedtopically to treat skin infectionsmade of a polycarbonate polymer that could help finish the job started byantibiotics. Once these polymers, which are 200 nanometers across, come into contact with water insidethe body or on the skin, they would self-assemble into a new polymer structure designed to targetbacteria-infected cells and lyse (disintegrate) their cell membranes and walls. These nanoparticlesdistinguish between healthy cells and bacteria-infected cells by the electric charges each produces. "The[electric] charge of these bacterial membranes is significantly higher than that of a healthy cell," Hedricksays. "We just tune the charge of the Nan particle to selectively go after the dangerous microbe. In theresearchers' in vitro testing they determined that even at levels 10-fold or higher than the normal dosing level, there is no rupturing of red blood cells, says Alan Louie, research director of IDC Health Insights, aFramingham, Mass,based consulting firm. Louie, who is familiar with but did not participate in the study,notes the importance of being able to "tune" the nanoparticles so that they stay in the body long enoughto do their job without accumulating in internal organs. Whereas other nonmaterial have been proposed totransport drugs in the body or fight disease, the polycarbonate polymers that Hedrick's team is studyingwould later be broken down by enzymes in the body and thus less likely to accumulate. "After a shortperiod of time they revert back to an innocuous by-product with a very low molecular weight that caneasily be removed from the body,"heads". The researchers' next step is to broaden the types of bacteria that their nanoparticles can destroy. Rightnow, they are tuned to attack so-called "gram-positive" bacteria such as MRSA, yeast and fungi. Hedrickwants to create a more universal ally to antibiotics that can likewise target gram-negative bacteria such asEsherichia coli and salmonella. "What makes gram-negative bacteria so tricky is that you have a muchmore complex membrane that surrounds the microbe," Hedrick says. "We're beginning to understand howto navigate and disrupt those membranes." Other areas of study include tinkering with nanoparticles'shape (a more elongated design could more easily navigate the body) and materials that have a lowermolecular weight but pack the same punch."Clearly, there's a lot of work ahead, particularly in validating the safety in humans and determining anappropriate vehicle to be able to deliver the nanoparticles into the human body," Louie says. Yet inaddition to the direction Hedrick outlined, Louie sees a lot of potential to nanoparticles' ability to selfassemble, creating a structure that could someday deliver medicine into the body and play an evenbigger role in health care.

- Akshay Kumar

EE-4th Sem

4G NETWORKS

Traditional phone networks (2G cellular networks) such as GSM, used mainly for voice transmission, areessentially circuit-switched. 2.5G networks, such as GPRS, are an extension of 2G networks, in that theyuse circuit switching for voice and packet switching for data transmission. Circuit switched technologyrequires that the user be billed by airtime rather than the amount of data transmitted since thatbandwidth is reserved for the user. Packet switched technology utilizes bandwidth much moreefficiently, allowing each user's packets to compete for available bandwidth, and billing users for theamount of data transmitted. Thus a move towards using packet-switched, and therefore IP networks, isnatural.3G networks were proposed to eliminate many problems faced by 2G and 2.5G networks, like lowspeeds and incompatible technologies (TDMA/CDMA) in different countries. Expectations for 3G includedincreased bandwidth: 128 Kbps in a car, and 2Mbps in fixed applications. In theory, 3G would work overNorth American as well as European and Asian wireless air interfaces. In reality, the outlook for 3G isneither clear nor certain. Part of the problem is that network providers in Europe and North Americacurrently maintain separate standards' bodies (3GPP for Europe and Asia; 3GPP2 for North America).The standards' bodies mirror differences in air interface technologies. In addition there are financialquestions as well that cast a doubt over 3G's desirability. There is a concern that in many countries, 3Gwill never be deployed. This concern is grounded, in part, in the growing attraction of 4G wirelesstechnologies. A 4G or 4th generation network is the name given to an IP-based mobile system thatprovides access through a collection of radio interfaces .A 4G network promises seamlessroaming/handover and best connected service, combining multiple radio access interfaces (such asHIPERLAN, WLAN, Bluetooth, GPRS) into a single network that subscribers may use. With this feature,users will have access to different services & increased coverage.One bill with reduced total access cost, and more reliable wireless access even with the failure or loss ofone or more networks. At the moment, 4G is simply an initiative by R&D labs to move beyond thelimitations, and deal with the problems of 3G (which is having trouble meeting its promisedperformance and throughput).At the most general level, 4G architecture will include three basic areas ofconnectivity: Personal Area Networking (such as Bluetooth), local high-speed access points on thenetwork including wireless LAN technologies (such as IEEE 802.11 and HIPERLAN), and cellularconnectivity. Under this umbrella, 4G calls for a wide range of mobile devices that support global roaming.Each device will be able to interact with Internet-based information that will be modified on the fly for thenetwork being used by the device at that moment. In short, the roots of 4G networks lie in the idea ofpervasive computingOne bill with

reduced total access cost, and more reliable wireless access even withthe failure or loss of one or more networks. At the moment, 4G is simply an initiative by R&D labs to movebeyond the limitations, and deal with the problems of 3G (which is having trouble meeting itspromised performance and throughput).At the most general level, 4G architecture will include three basic areas of connectivity: Personal Area Networking (such as Bluetooth), local high-speed access points onthe network including wireless LAN technologies (such as IEEE 802.11 and HIPERLAN), and cellularconnectivity. Under this umbrella, 4G calls for a wide range of mobile devices that support global roaming.Each device will be able to interact with Internet-based information that will be modified on the fly for thenetwork being used by the device at that moment. In short, the roots of 4G networks lie in the idea ofpervasive computing. The glue for all this is likely to be software defined radio (SDR). SDR enablesdevices such as cell phones, PCs and a whole range of other devices to scan the airwaves for the bestpossible method of connectivity, at the best price. In an SDR environment, functions that wereformerly carried out solely in hardware - such as the generation of the transmitted radio signal and the tuning of the received radio signal - are performed by software. Thus, the radio is programmable andable to transmit and receive over a wide range of frequencies while emulating virtually any desiredtransmission format.

4G Characteristics

The defining features of 4G networks are listed below:

- High Speed 4G systems should offer a peak speed of more than 100Mbits per second in stationary mode with an average of 20Mbits per second when traveling.
- High Network capacity - Should be at least 10 times that of 3G systems.

This will quicken the download time of a 10-Mbyte file to one second on4G, from 200 seconds on 3G, enabling high-definition video to stream to phones and create a virtual reality experience on high-resolution handset screens.Fast/Seamless handover across multiple networks 4G wireless networks should support globalroaming across multiple wireless and mobile network.Next-generation multimedia support - The underlying network for 4G must be able to support fastspeed and large volume data transmission at a lower cost than today.

- Swati

EE-7thSem

3-D ICs

There is a saying in real estate; when land gets expensive, multi-storied Buildings is the alternative

solution. We have a similar situation in the chip Industry. For the past thirty years, chip designers haveconsidered whether Building integrated circuits multiple layers might create cheaper, more powerfulChips. Performance of deep-sub micrometer very large scale integrated (VLSI) Circuits is beingincreasingly dominated by the interconnects due to increasing wire pitch and increasing die size.Additionally, heterogeneous integration of different technologies on one single chip is becomingincreasingly desirable, for which planar (2-D) ICs may not be suitable. The three dimensional (3-D) chipdesign strategy exploits the vertical dimension to alleviate the interconnect related problems and tofacilitate heterogeneous integration of technologies to realize system on a chip (SoC) Design. By simplydividing a planar chip into separate blocks, each occupying separate physical level interconnected byshort and vertical interlayer Interconnects (VILICs), significant improvement in performance and reductionin wire-limited chip area can be achieved. In the 3-Ddesign architecture, an entire chip is divided into anumber of blocks, and each block is placed on a separate layer of Si that are stacked on top of eachother.

MOTIVATION FOR 3-D ICs

The unprecedented growth of the computer and the information technology industry is demanding VeryLarge Scale Integrated (VLSI) circuits with increasing functionality and performance at minimum cost andpower dissipation. Continuous scaling of VLSI circuits is reducing gate delays but rapidly increasinginterconnects delays. A significant fraction of the total power consumption can be due to the wiringnetwork used for clock distribution, which is usually realized using long global wires. Furthermore,increasing drive for the integration of disparate signals (digital, analog, RF) and technologies (SOI, SiGe,GaAs, and so on) is introducing various SoC design concepts, for which existing planner (2-D) IC Designmay not be suitable.

- Naveen Kumar
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Asynchronous Chips

Computer chips of today are synchronous. They contain a main clock, which controls the timing of theentire chips. There are problems; however, involved with these clocked designs that are common today.One problem is speed. A chip can only work as fast as its slowest component. Therefore, if one part of thechip is especially slow, the other parts of the chip are forced to sit idle. This wasted computed time isobviously detrimental to the speed of the chip. New problems

with speeding up a clocked chip are justaround the corner. Clock frequencies are getting so fast that signals can barely cross the chip in oneclock cycle. When we get to the point where the clock cannot drive the entire chip, we'll be forced to come up with a solution. One possible solution is a second clock, but this will incur overhead and powerconsumption, so this is a poor solution. It is also important to note that doubling the frequency of the clockdoes not double the chip speed, therefore blindly trying to increase chip speed by increasing frequencywithout considering other options is foolish. The other major problem with clocked design is powerconsumption.The clock consumes more power that any other component of the chip. The most disturbing thing aboutthis is that the clock serves no direct computational use. A clock does not perform operations oninformation; it simply orchestrates the computational parts of the computer. New problems with power consumption are arising. As the number of transistors on a chi increases, so does the power used by theclock. Therefore, as web design more complicated chips, power consumption becomes an even morecrucial topic. Mobile electronics are the target for many chips. These chips need to be even more conservative with power consumption in order to have a reasonable battery lifetime. The natural solutionto the above problems, as you may have guessed, is to eliminate the source of these headaches: theclock. The Caltech Asynchronous Microprocessor is the world's first asynchronous microprocessor(1989).Asynchronous, or clock less; design has advantages over the synchronous design. The first ofthese advantages is speed. Chips can run at the average speed of all its components instead of thespeed of its slowest component, as was the case with a clocked design. Also the need to have a clockrunning at a speed such that the signal can reach all parts of the chip is eliminated. Therefore, the speedof an asynchronous design is not limited by the size of the chip. An example of how much anasynchronous design can improve speed is the asynchronous Pentium designed by Intel in 1997 thatruns three times as fast as the synchronous equivalent. This speedup is certainly significant and provesthe usefulness of a clock less design. The other advantage of a clock less design is power consumption.Special light emission measurements of a synchronous chip (left) and an asynchronous chip (right) withthe same digital functionality under the same operational conditions indicate how much power the chips dissipate.

The above graphic illustrates the power saving characteristic of a clock less design. The reason for this isthat asynchronous chips use power only during computations, while a clocked chip always consumespower because the chip is always running. Remember that the clock is the

component which consumesthe most power. Therefore, eliminating the clock eliminates the largest component of power consumption.One example of improved power consumption is the same Intel Pentium asynchronous chip. This design,which ran up to three times as fast as the clocked version, runs on half the power of the clocked version.This is incredible support for a clock less design. A second example of improved power consumption is a Philips prototype chip that runs on one-third of the power of its clocked counterpart. Clock less design isinevitable in the future of chip design because of the two major advantages of speed and powerconsumption, but where will we first see these designs in use? The first place we'll see, and have alreadyseen, clock less designs are in the lab. Many prototypes will be necessary to create reliable designs.Manufacturing techniques must also be improved so the chips can be mass-produced. The second placewe'll see these chips are in mobile electronics. This is an ideal place to implement a clock less chipbecause of the minimal power consumption. Also, low levels of electromagnetic noise creates lessinterference, less interference is critical in designs with many components packed very tightly, as is thecase with mobile electronics. The third place is in personal computers (PCs). Clock less designs will occurhere last because of the competitive PC market. It is essential in that market to create an efficient designthat is reasonably priced. A manufacturing cost increase of a couple of cents per chip can cause an entireline of computers to fail because of the large cost increase passed onto the customer. Therefore, themanufacturing process must be improved to create a reasonably priced chip. A final place thatasynchronous design may be used is encryption devices. The reason for this is there are no regularlytimed signals for hackers to look for. This becomes even more critical as computers all over the worldbecome more closely connected and are sharing confidential material. Security in the United States hasincreased greatly in rEEnt times; therefore, a clock less design will be welcomed because of itsencryption abilities. In summary, clock less designs have limitations, specifically a limited speed and highpower consumption. Fortunately, these limitations can be solved with a clock less design. These

asynchronous designs will be seen in many areas of technology, but it will take time before these chipscan be perfected. Conventional chips operate under the control of a central clock, which samples data inthe registers at precisely timed intervals. clock less chips dispense with the timepiEE. In one scheme,data moves instead under the control of local “handshake” signals that indicate when work has beencompleted and is ready for the next logic operation.

- Taranjit Kaur
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Some Interesting Quotes On Electronics

Electronic mail has been a huge phenomenon for us. It gives us a little bit of a closer feel. Even ifsomebody's office is in another building, you're always sending them some messages. And even ifthey're off in another country it makes that easy. -BILL GATESElectronic calculators can solve problems which the man who made them cannot Solve, -JOSEPHWOODS KRUTCHIn this electronic age we see ourselves being translated more and more into the form of information,moving toward the technological extension of consciousness. -MARSHALL MCLUHANStates had to also have electronic voting machines that made it possible for people who arephysically handicapped to vote in private... and the computerized voting machine made it very easyfor, particularly, the blind -DEFOREST SORIES *Certainly the advent of technology and electroniccommerce had an immense impact on the real estate industry. -MICHAEL OX

- Taresh

EE- 8th sem

Riddles

1. I have holes in my top and bottom, my left and right, and in the middle. But I still hold water. What am I?
2. I am weightless, but you can see me. Put me in a bucket, and I'll make it lighter. What am I?
3. I'm light as a feather, yet the strongest man can't hold me for much more than a minute. What am I?
4. I'm the part of the bird that's not in the sky. I can swim in the ocean and yet remain dry. What am I?
5. Throw it off the highest building, and I'll not break. But put me in the ocean, and I will. What aml?
6. I run over fields and woods all day. Under the bed at night I sit not alone. My tongue hangs out, upand to the rear, waiting to be filled in the morning. What am I?
7. A certain crime is punishable if attempted but not punishable if committed. What is it? - Suicide
8. The man who invented it doesn't want it. The man who bought it doesn't need it. The man who needsit doesn't know it. What is it?

9. You use a knife to slice my head and weep beside me when I am dead. What am I?

10. You throw away the outside and cook the inside. Then you eat the outside and throw away the inside.What did you eat?

SOLUTION:

1. Sponge 2.A hole 3. Breath 4. Shadow 5. Waves 6. Shoe 7. Suicide 8. Coffin 9. Onion 10. Chicken E

- Deepak gupta
EE-6th sem

Gems of Era

Archimedes (c. 287 BC c. 212 BC)

Archimedes was a great mathematician,physicist, engineer, inventor, andastronomer of his age. But generally, heis considered to be the greatestmathematician of antiquity and one of thegreatest of all time.

Andreas Vesalius (1514-1564

Andreas Vesalius was an anatomist,physician, and also an author of one ofthe most influential books on humananatomy. He is considering as the—founder of modern human anatomy ‖ .His important innovations were toperform postmortem dissections.

Technical Jokes

1) A retired electronic technician came into the clinic and said, "Doctor, I have a serious memory problem." Thedoctor asked, **"When did it start?"** The technician replied, **"When did what start?"**

2) An Engineer working in the film factory came running in the office and yelled, "Doctor, doctor!! - my colleaguejust swallowed a roll of film!!" The doctor calmly replied, **"Let's just wait and see what develops."**

3) When I told my doctor I broke my leg in two places while carrying a big Monitor, he told me to stop going tothose places.

4) I told my repair friend I had a ringing in my ears due to the heavy explosion caused by a big capacitor. Hisadvice: **"Don't answer it."**

GOLDEN PHRASES

Money glitters, beauty sparkles, and intelligence shines. - *Hitler*
When there is a conflict between heart & brain let the heart be followed. -*Swami Vivekananda*

“There is a time to let things happen and a time to make things happen.” - *Hugh Prather*

“Sometimes you win and sometimes you learn.” - *Kiyosak*

“One day in retrospect the years of struggle will strike you as the most beautiful.”

- *Sigmund Freud*

“Success often comes to those who have the aptitude to see way down the road.”

- *Laing Burns, Jr.*

The secret of life is not enjoyment, but education through experience Without continual growth and progress, suchwords as improvement, achievement, and success have no meaning.

- *Benjamin Franklin*

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